PCL-1800

High-speed
DAS card with
programmable gain

Acknowledgments
PC-LabCard is a trademark of Advantech Co., Ltd. IBM and PC are trademarks of International Business Machines Corporation. MS-DOS, Microsoft C and QuickBASIC are trademarks of Microsoft Corporation. BASIC is a trademark of Dartmouth College. Intel is a trademark of Intel Corporation. TURBO C is a trademark of Borland International.

Part No. 2003180020 2nd Edition
Printed in Taiwan March 1995

Contents

CHAPTER 1

General information

Introduction

The PCL-1800 is a very-high-speed, high-performance multifunction plug-in DAS card for the IBM PC/AT and compatible computers. It features a 330 KHz 12-bit analog-to-digital converter, on board 1 K word FIFO buffer, two 12-bit D/A output channels, 16 digital input channels, 16 digital output channels and one 16-bit counter channel.

The PCL-1800 also includes a 16-channel, 8-bit analog comparator which you can use as an analog watchdog to monitor the card's 16 analog input signals. If a signal goes above or below a triggering value, the PCL-1800 can generate an interrupt and transfer data.

The card provides DMA data transfer on one of its two 12-bit D/A output channels. This channel lets you perform synchronous data output at up to 200 KHz, excellent for waveform generation.

All these sophisticated functions make the PCL-1800 an ideal data acquisition system for your laboratory applications which require very-high speed and powerful triggering capabilities.

In addition to the high performance hardware a new enhanced version of PC-Scope is also included. PC-Scope turns your computer into a menu driven digital storage oscilloscope. This program allows users to easily perform pre- and post-trigger high speed data acquisition. The collected data can be stored on to disk or be analyzed by the FFT (Fast Fowier Transform) function.

Features

- 330 KHz 12-bit A/D converter
- 16 single-ended or eight differential inputs
- Built-in 1 K word FIFO buffer
- 16-channel analog comparator
- 330 KHz data transfer rate with FIFO
- 200 KHz data transfer rate with DMA
- 12-bit analog output with DMA

- Unipolar/bipolar input with programmable gain
- 16 digital inputs and 16 digital outputs
- Furnished with menu-driven scope software package

Analog input

The PCL-1800 features a 12-bit high-speed A/D converter with 2.5 msec. conversion time. It also includes an on-board sample-and-hold circuit with software programmable input range. You can trigger the A/D conversion from your program, the on-board programmable pacer or an external trigger.

The PCL-1800 can select either eight differential or 16 single ended analog inputs by switch. Like Advantech's other high-performance cards the PCL-1800 offers auto-channel/gain scanning. This feature allows high-speed multichannel sampling with DMA (up to 200 KHz) and different gain for each channel.

On-board 1 K word FIFO with programmable index

To increase the throughput and improve performance under Windows the PCL-1800 includes a 1 K word FIFO (First In First Out) buffer. A programmable index with one-step resolution lets you acquire anywhere from one to 1024 analog-to-digital-conversion data elements at a time. For example, if you set the FIFO's index to 25, after the card completes 25 A/D conversions, it will generate an interrupt and transfer just 25 data elements. You don't need to wait until the FIFO is full or half-full to receive your data.

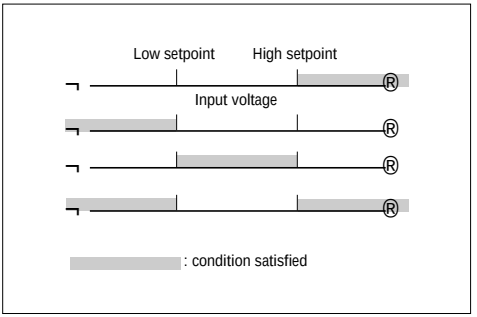
Data transfer

The PCL-1800 can transfer the A/D conversion data in four different ways: software polling, interrupt service routine, DMA and FIFO. The method you use determines the speed of the data transfer, as shown below:

Method	Max. A/D throughput
Software polling	10-20 KHz (depending on PC speed)
Interrupt	10-30 KHz
DMA	200 KHz
FIFO w/repeat input string	330 KHz

16-channel analog watchdog

The PCL-1800's special watchdog circuit lets you precisely monitor the analog input lines. Two 8-bit comparators on each input line store the desired values and compare the values against the reading on the input line. The watchdog circuit reads the result of the comparators and triggers an interrupt. You can set each comparator individually to trigger if the line reading is above or below its desired value, and you can set the watchdog to trigger on any combination of comparator readings.



Analog watchdog trigger conditions

This control logic (all software programmable) lets you set up complex alarming and triggering conditions. For example, you can set the watchdog to trigger if the input is either above the high-level value or below the low-level value. Using the software driver you can combine the PCL-1800's FIFO and watchdog to perform pre-, post- and position-triggering.

Analog output

The PCL-1800 provides two 12-bit analog output channels, one with DMA transfer capability. The PCL-1800 can achieve up to 200 KHz throughput. It can also perform waveform storage and playback. Analog output ranges are 0 ~ 5 V or 0 ~ 10 V with internal reference and ±10 V max. with external reference.

Specifications

Analog input

- **Channels**: 16 single ended, eight differential (selectable)
- **Resolution**: 12 bit
- **Conversion time**: 3 msec
- **Input ranges**:
  Bipolar: ±10 V, ±5 V, ±2.5 V, ±1.25 V and ±0.625 V
  Unipolar: 0~10 V, 0~5 V, 0~2.5 V and 0~1.25 V
- **Automatic channel gain/scan**
- **Trigger modes**:
  Software, pacer or external trigger pre-, post- and position-triggering
- **Data transfer**:
  Program-controlled, interrupt (IRQ 2, 4, 5, 7, 10, 11, 12 or 15) or 16-bit DMA transfer (DRQ 5 to 7) selected by software
- **FIFO size**: 1 K word
- **Data transfer rate**: 200 KHz with DMA
  330 KHz with FIFO
- **Accuracy**: 0.01% of FSR ±1 LSB
- **Temperature coefficient**: 25 PPM/°C

Analog output

- **D/A channel**: Two 12-bit channels, one with DMA transfer
- **D/A range**: 0 to 5 V or 0 to 10 V with internal reference
  10 V max. with external reference
- **Setting time**: 5 msec. max. on channel 1
- **D/A pacer rate**: 200 KHz max. (DMA channel only)
- **Output current**: ±5 mA
- **Data transfer**:
  channel 0 s/w control only
  channel 1 s/w or 16-bit DMA control
- **Accuracy**: ±0.01% FSR
- **Linearity**: ±½ LSB max.

Digital input

- **Channel**: 16 bits
- **Low voltage**: 0.8 V max.
- **High voltage**: 2.0 V min.

Digital output

- **Channel**: 16 bits
- **Low voltage**: 0.4 V max. @ 16 mA (sink)
- **High voltage**: 2.4 min. @ 0.8 mA (sink)

Counter and A/D pacer rate

- **Device**: 8254
- **Pacer rate**: 2.5 MHz to 0.00023 Hz
  (one cycle every 72 minutes), software programmable
- **Counter**: One 16-bit counter with 100 KHz time base

Interrupt channel

- Level: IRQ 2, 4, 5, 7, 10, 11, 12 or 15
- Enabling: Software controlled

DMA channel

- Level: 5, 6, 7
- Enabling: Software controlled

FIFO

- **Size**: 1 K words (2 K words optional)
- **Bus**: 16 bits (12 data, 4 channel number)
- **Flags**: Full, half-full, empty
- **Reset**: Strobe BASE+30

Watchdog comparators

- **Channels**: 16 (one for each input channel)
- **Conditions**: Above, below, in-between and above/below
- **Enabling**: Software controlled

Down counter

- **Bits**: 11
- **Load**: Auto-reload when count is finished

General

- **I/O port**: 32 consecutive bytes
- **Bus**: 16-bit ISA (AT)
- **Dimensions**: 4.8" x 8.6" (122 mm x 218 mm)
- **Power consumption**: +5 V @ 600 mA max.;
  +12 V @ 200 mA max.; -12 V @ 15 mA typical

Daughterboards

We offer a wide variety of optional daughterboards to help you get the most from your PCL-1800. You will need the PCLD-774 Analog Expansion Board or PCLD-8115 Wiring Terminal Board to make connections.

- **PCLD-787 8-channel simultaneous sample and hold board**
This board lets you simultaneously acquire up to eight analog inputs with less than 30 nsec. of channel-to-channel sample time uncertainty.

- **PCLD-786 AC/DC power SSR and relay driver board**
This board holds eight opto-isolated solid state relay modules and provides an additional eight outputs to drive external relays.

- **PCLD-785B and PCLD-885 relay output boards**
These boards let you control relays through the PCL-1800's 16-bit digital output channels. PCLD-785B provides 24 SPDT relays, while the PCLD-885 provides 16 SPST power relays.

- **PCLD-782B Isolated D/I Board**
This board provides 24 opto-isolated digital input channels and a cable to connect to the PCL-1800's digital input ports.

- **PCLD-5B16 module carrier board**
This board holds 16 5B-series input and/or output modules. We supply 5B modules for wide variety of signal input signals, including thermocouples, strain gauges and RTDs.

Software support

The PCL-1800 comes with a powerful and easy-to-use software driver whose functions can be accessed by referring to a user-defined Parameter Table. With these driver functions your application programming becomes much easier, especially when you want to use some of the sophisticated features available from the PCL-1800, such as interrupt or DMA data transfer. Refer to the software driver user's manual for details.

The following Advantech application software products support the PCL-1800, or will support it in the near future. Contact your local representative for details.

- **DAXpert**

DOS-based general purpose data acquisition package. You can quickly set up an experiment, acquire data and graphically display the results on the screen in real time.

- **GENIE**

Windows-based general purpose data acquisition package. Its intuitive, object-oriented graphical user interface simplifies control strategy and display setups.

- **DLL driver**

You can use this DLL driver to program your card under Microsoft Windows.

- **PC-Scope, special PCL-1800**

This software turns your PC into a storage-oscilloscope. This special version takes full advantage of the PCL-1800's features.

A number of popular 3rd-party software companies will also support the PCL-1800, depending on their own schedules. Contact your local representative for details. Software packages include:

- LABTECH NOTEBOOK
- LABTECH NOTEBOOKpro
- LABTECH CONTROL
- LABTECH CONTROLpro
- DASYLab
- DADiSP/PRO-32
- SNAP-MASTER for Windows

CHAPTER 2

Installation

Initial inspection

We carefully inspected the PCL-1800 both mechanically and electrically before we shipped it. It should be free of marks and scratches and in perfect order on receipt.

As you unpack the PCL-1800, check it for signs of shipping damage (damaged box, scratches, dents, etc.). It is damaged or fails to meet specifications, notify our service department or your local sales representative immediately. Also, call the carrier immediately and retain the shipping carton and packing material for inspection by the carrier. We will then make arrangements to repair or replace the unit.

Discharge any static electricity on your body before you touch the board by touching the back of the system unit (grounded metal).

Remove the PCL-1800 card from its protective packaging by grasping the rear metal panel. Handle the card only by its edges to avoid static electric discharge which could damage its integrated circuits. Keep the antistatic package. Whenever you remove the card from the PC, store the card in this package for protection.

You should also avoid contact with materials that hold static electricity such as plastic, vinyl and styrofoam.

Switch and jumper settings

You set the basic configuration of the PCL-1800 through two function switches and four jumpers, as summarized in the following table:

Option	Setting
Channel configuration, S. E. or diff.	SW1
Base address selection	SW2
Internal voltage reference, -10 V or -5 V	JP1
TRIG0 and GATE0 Selection	JP2
D/A reference voltage, int./ext.	JP3, JP4

You may want to refer to the figure in Appendix B for help identifying card components.

Channel configuration, S. E. or diff. (SW1)

The PCL-1800 offers 16 single-ended or eight differential analog input channels. SW1 changes the channels between single-ended or differential input. Slide the switch to the upper position, marked DIFF, for eight differential inputs. Slide the switch to the upper position, marked S/E, for 16 single ended inputs. DIFF is the default.

Single-ended inputs

Differential inputs (default)

Base address selection (SW2)

You control the PCL-1800's operation by reading or writing data to the PC's I/O (input/output) port addresses. The PCL-1800 requires 32 consecutive address locations. Switch SW2 sets the card's base (beginning) address. Valid base addresses range from Hex 000 to Hex 3F0. Other devices in your system may, however, be using some of these addresses.

We set the PCL-1800 for a base address of Hex 300 at the factory. If you need to adjust it to some other address range, set switch SW2 as shown in the following table:

Card I/O addresses (SW2)

Range (hex)	Switch position					
	1	2	3	4	5	6
000 - 01F	●	●	●	●	●	●
200 - 21F	○	●	●	●	●	●
*300 - 31F	○	○	●	●	●	●

○ = Off ● = On * = default

Note: Switches 1-5 control the PC bus address lines as follows:

Switch	1	2	3	4	5	6
Line	A9	A8	A7	A6	A5	A4

In this line A4 is not useful.

Appendix C provides a PC I/O port address map to help you avoid conflicts the I/O addresses for standard PC devices.

Internal voltage reference, -10 V or -5 V (JP1)

The PCL-1800 gives you a choice of DC internal reference voltage sources: -5 V and -10 V. To use internal reference you will need to set jumpers JP3 and JP4. Both D/A output channels will use the same reference voltage.

Jumper settings appear below:

-10 V

-5 V (default)

TRIG0 and GATE0 Selection (JP2)

JP2 has two jumpers. The upper jumper selects the card's A/D trigger source when you use external triggering. The lower jumper selects the gate control for counter 0 of the card's 8254 timer/counter.

Upper jumper – Source for external trigger:

You have two choices: DI0 (pin 1) on connector CN2 or TRIG0 (pin 35) on CN3.

TRIG0

DI0 (default)

Either choice selects external triggering.

Lower jumper – Counter 0 gate controller

You have two choices: DI2 (pin 3) on connector CN2 or GATE0 (pin 36) on CN3.

GATE0

DI2 (default)

We recommend that you leave JP2 set to the default DI0 and DI2 (both jumpers in the left-hand position), because this setting is required by the software driver. This setting has the same effect as that achieved by SW6 positions 7 and 8 on the PCL-718 card.

D/A reference voltage, int./ext. (JP3, JP4)

Jumpers JP3 and JP4 select the reference voltage source for the PCL-1800's two D/A converter channels. You can use the card's internal reference or supply an external reference. JP3 controls channel 0, and JP4 controls channel 1. Jumper settings are as follows:

JP3 = channel 0
JP4 = channel 1

External ref.

Internal ref. (default)

When you set a D/A channel's jumper to INT, the channel takes its reference voltage input from the card's on-board reference. Jumper JP1 sets the on-board reference to either -5 V or -10 V. With the jumper set to INT, the D/A channel then has an output range of 0 V to +5 V or 0 V to +10 V.

When you set the channel's jumper to EXT, the D/A converter takes its reference voltage input from connector CN3 pin 31 (for channel 0) or pin 12 (for channel 1). You can apply any voltage between -10 V and +10 V to function as the external reference. The reference input can be either DC or AC (< 100 KHz).

When you use an external reference with voltage V_{ref}, you can program the D/A channel to output from 0 V to $-V_{ref}$. You can also use the D/A converter as a programmable attenuator. The attenuation factor between reference input and analog output is:

Attenuation factor = G / 4095

where G is a value you write to the D/A registers between 0 and 4095. For example, if you set G to 2048, then the attenuation factor is 0.5. A sine wave of 10 V amplitude applied to the reference input will generate a sine wave of 5 V amplitude on the analog output.

For more information on using the D/A output, see page 61.

Connector pin assignments

The PCL-1800 has two on-board 20-pin flat-cable connectors (insulation displacement, mass termination) and a DB-37 connector accessible from the card bracket. See the figure in Appendix B for the location of each connector.

Pin assignments for each connector appear in the following sections.

Abbreviations	
A/D S	Analog input (single-ended)
A/D H	Analog input high (differential)
A/D L	Analog input low (differential)
A.GND	Analog ground
D/A	Analog output
D/O	Digital output
D/I	Digital input
D.GND	Digital and power supply ground
CLK	Clock input for the 8254
GATE	Gate input for the 8254
OUT	Signal output of the 8254
VREF	Internal voltage reference
REFIN	External voltage reference input
D/A ECLK	D/A external clock input
A/D EXT TRIG	A/D external pacer input

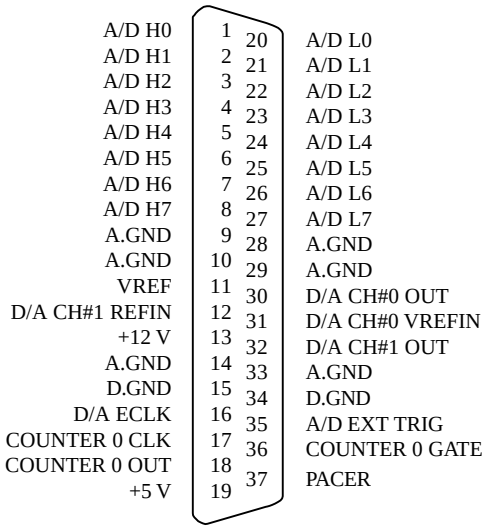
Connector CN1 – Digital output

D/O 0	1	2	D/O 1
D/O 2	3	4	D/O 3
D/O 4	5	6	D/O 5
D/O 6	7	8	D/O 7
D/O 8	9	10	D/O 9
D/O 10	11	12	D/O 11
D/O 12	13	14	D/O 13
D/O 14	15	16	D/O 15
D.GND	17	18	D.GND
+5 V	19	20	+12 V

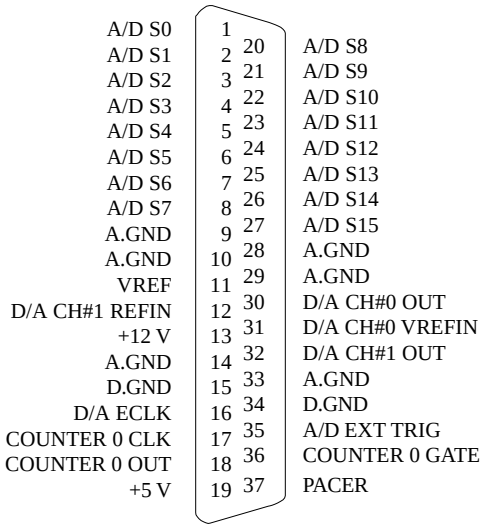
Connector CN2 — Digital input

D/I 0	1	2	D/I 1
D/I 2	3	4	D/I 3
D/I 4	5	6	D/I 5
D/I 6	7	8	D/I 7
D/I 8	9	10	D/I 9
D/I 10	11	12	D/I 11
D/I 12	13	14	D/I 13
D/I 14	15	16	D/I 15
D.GND	17	18	D.GND
+5 V	19	20	+12 V

Connector CN3 – Analog input/output/counter, Differential operation



Connector CN3 – Analog input/output/counter, Single-ended operation



Hardware installation

Warning! *Disconnect power from the PC whenever you install or remove the PCL-1800 or its cables.*

Installing the card in your computer

1. Turn the computer off. Turn the power off to any peripheral devices such as printers and monitors.
2. Disconnect the power cord and any other cables from the back of the computer.
3. Remove the system unit cover (see the user's guide for your chassis if necessary).
4. Locate the expansion slots at the rear of the unit and choose any unused slot.
5. Remove the screw that secures the expansion slot cover to the system unit. Save the screw to secure the interface card retaining bracket.
6. Carefully grasp the upper edge of the PCL-1800 card. Align the hole in the retaining bracket with the hole on top of the expansion slot and align the gold striped edge connector with the expansion slot socket. Press the board firmly into the socket.
7. Secure the PCL-1800 using the screw you removed in step 5.
8. Attach any accessories (using DB-37 cable, etc.) to the PCL-1800.
9. Replace the system unit cover. Connect the cables you removed in step 2. Turn the computer power on.

Hardware installation is now complete. Install the software driver as described in the following section.

Software installation

The PCL-1800 includes a floppy disk with utility software. The disk contains the following:

1. A comprehensive I/O driver for A/D, D/A, digital I/O and counter applications. This driver lets you operate the PCL-1800 using high-level programming languages. You do not need to perform detailed register programming. The driver supports the following languages: BASICA, GWBASIC, QUICKBASIC, Microsoft C/C++ and PASCAL, Turbo C/C++, Borland C/C++ and Turbo PASCAL. Please refer to the Software Driver User's Manual for more information.
2. Demonstration programs
3. A calibration program
4. Test programs
5. Register level, direct I/O command Demo Program
6. PC-Scope for PCL-1800

We strongly recommend that you make a working copy from the master disk and store the master disk in a safe place. You can use the DOS COPY or DISKCOPY commands to copy the disk files to another floppy disk or simply use the COPY command to copy the files to a hard disk.

CHAPTER 3

Signal connections

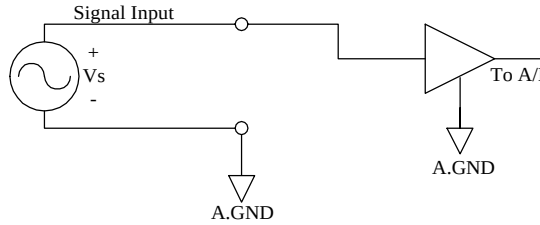
Correct signal connections are one of the most important factors to consider if your application is to send and receive data with accuracy. Good signal connections can also avoid a lot of unnecessary damage to your valuable PC and other hardware. This chapter provides information on signal connections for different types of data acquisition applications.

Analog input connections

The PCL-1800 supports either 16 single-ended or 8 differential analog inputs. Switch SW1 selects the input channel configuration.

Single-ended channel connections

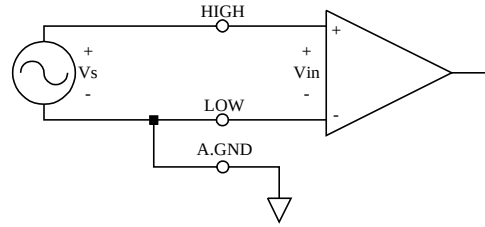
Single-ended connections use only one signal wire per channel. The voltage on the line references to the common ground on the card. A signal source without a local ground is called a “floating” source. It is fairly simple to connect a single ended channel to a floating signal source. A standard wiring diagram looks like this:



Differential channel connection

Differential input connections use two signal wires per channel. The card measures only the voltage difference between these two wires, the HI wire and the LOW wire. If the signal source has no connection to ground, it is called a “floating” source. A connection must exist

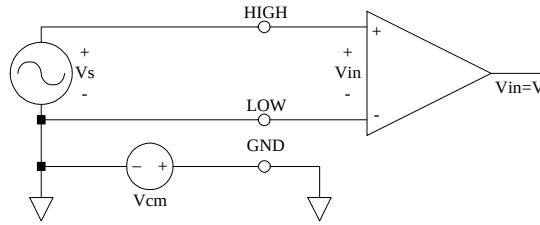
between LOW and ground to define a common reference point for floating signal sources. To measure a floating source connect the input channel as shown below:



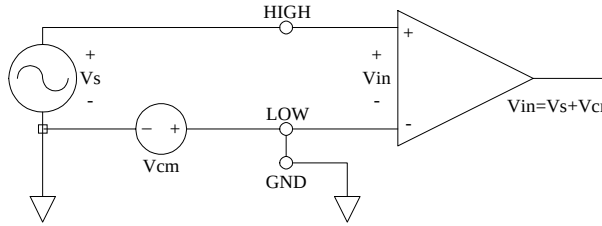
If the signal source has one side connected to a local ground, the signal source ground and the PCL-1800 ground will not be at exactly the same voltage, as they are connected through the ground return of the equipment and building wiring. The difference between the ground voltages forms a common-mode voltage.

To avoid the ground loop noise effect caused by common-mode voltages, connect the signal ground to the LOW input. Do not connect the LOW input to the PCL-1800 ground directly. In some cases you may also need a wire connection between the PCL-1800 ground and the signal source ground for better grounding. The following two diagrams show correct and incorrect connections for a differential input with local ground:

Correct connection



Incorrect connection



Expanding analog inputs

You can expand any or all of the PCL-1800's A/D input channels using multiplexing daughterboards. Most daughterboards require the PCLD-774 Analog Expansion Board or the PCLD-8115 Screw Terminal Board for connections.

The PCLD-789 Amplifier and Multiplexer multiplexes 16 differential inputs to one A/D input channel. You can cascade up to eight PCLD-789s to the PCL-1800 for a total of 128 channels. See the PCLD-779 user's manual for complete operating instructions.

The PCLD-774 Analog Expansion Board accommodates multiple external signal-conditioning daughterboards, such as PCLD-779 and PCLD-789. It features five sets of on-board 20-pin header connectors. A special star-type architecture lets you cascade multiple signal-conditioning boards without the signal-attenuation and current-loading problems of normal cascading.

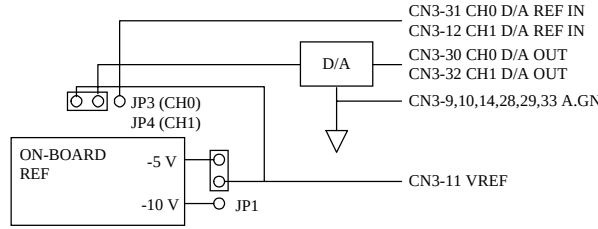
The PCLD-8115 Screw Terminal Board makes wiring connections easy. It provides 20-pin flat cable and DB-37 cable connectors. It also includes CJC (Cold Junction Compensation) circuits which let you directly measure thermocouples with your PCL-1800. You can handle all types of thermocouples with software compensation and linearization.

Special circuit pads on the PCLD-8115 accommodate passive signal conditioning components. You can easily implement a low-pass filter, attenuator or current shunt by adding resistors and capacitors.

Analog output connection

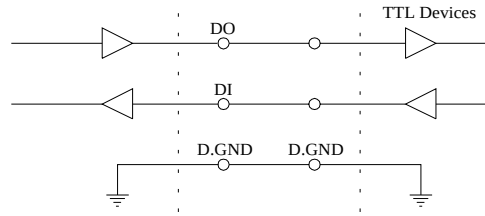
The PCL-1800 provides two D/A output channels. You can use the internal precision -5 V or -10 V reference to generate 0 to +5 V or 0 to +10 V D/A output. Use an external reference for other D/A output ranges. The maximum reference input voltage is ±10 V and maximum output scaling is ±10 V. Loading current for D/A outputs should not exceed 5 mA.

Connector CN3 provides D/A signals. Important D/A signal connections such as input reference, D/A outputs and analog ground appear below:

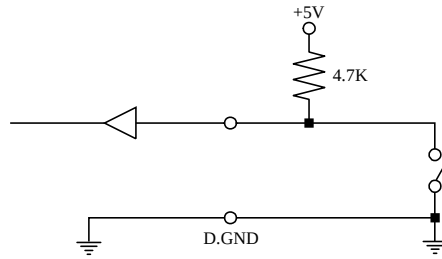


Digital signal connections

The PCL-1800 has 16 digital input and 16 digital output channels. The digital I/O levels are TTL compatible. The following figure shows connections to exchange digital signals with other TTL devices:



To receive an OPEN/SHORT signal from a switch or relay, add a pull-up resistor to ensure that the input is held at a high level when the contacts are open. See the figure below:



CHAPTER 4

Register structure and format

This chapter shows the format for each of the PCL-1800's registers.

Register-level programming for the card's more advanced functions, such DMA data transfer or pre-triggering, is extremely complicated. In practice you will need to use the card's software driver. We provide the register layout information only to help you understand what the functions in the software driver are doing.

On the other hand, register layout and programming for most of the card's standard functions, such as digital I/O, are the same as for other cards in the PCL-818 Series. Any programs you have written which directly access the registers should work with few modifications.

Notes in the text indicate functions which require the software driver.

Register format

The PCL-1800 requires 32 consecutive addresses in the PC's I/O space. Each address corresponds to a card register. The address of each register is specified as an offset from the card's base address. For example, BASE+0 is the card's base address, and BASE+7 is the base address + seven bytes. Read address BASE+0 (A/D conversion data) and write address BASE+26 (D/A output channel 1 data) are 16-bit access. All other addresses are 8-bit access.

I/O port address map

The following table shows the function of each register or driver and its address relative to the card's base address.

I/O port address assignments

Address	Read	Write
BASE+0	A/D data and channel (16-bit)	Software A/D trigger
BASE+1	N/A	A/D range control
BASE+2	MUX scan channel	MUX scan channel and range control pointer
BASE+3	D/I low byte (DI 0-7)	D/O low byte (DO 0-7)
BASE+4	N/A	D/A 0 low byte
BASE+5	N/A	D/A 0 high byte
BASE+6	N/A	N/A
BASE+7	N/A	N/A
BASE+8	A/D status	Clear A/D interrupt request
BASE+9	Control	Control
BASE+10	N/A	Timer/counter enable
BASE+11	D/I high byte (DI 8-15)	D/O high byte (DO 8-15)
BASE+12	Counter 0	Counter 0
BASE+13	Counter 1	Counter 1
BASE+14	Counter 2	Counter 2
BASE+15	N/A	Counter control
BASE+16	N/A	Watchdog comparator (8-bit)
BASE+17	N/A	Watchdog comparator
BASE+18	N/A	Watchdog comparator
BASE+19	N/A	Clear watchdog
BASE+20	N/A	N/A
BASE+21	Status	PCL-1800 mode control
BASE+22	Status	Function control
BASE+23	Status	DMA and IRQ selection
BASE+24	Ch. no. which matches watchdog condition	Time base selection

Address	Read	Write
BASE+25	N/A	Strobe channel number to latch watchdog
BASE+26	N/A	16-bit D/A data (DA 1)
BASE+27	N/A	N/A
BASE+28	Clear down-counter flag	Down-counter low byte
BASE+29	N/A	Down-counter high byte
BASE+30	Card ID code	Reset FIFO

BASE + 0 (read) A/D data register

A 16-bit register at BASE+0 holds data from each A/D conversion and identifies the source A/D channel number. Bits 15 (MSB) to 4 (LSB) hold the 12 bits of data from the conversion. Bits 3 to 0 hold the source A/D channel number.

BASE + 0 A/D conversion data and channel number (read)								
Bit	D15	D14	D13	D12	D11	D10	D9	D8
Value	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	AD3	AD2	AD1	AD0	C3	C2	C1	C0

AD11 to AD0 Analog to digital conversion data. AD0 is the least significant bit (LSB) of the A/D data, and AD11 is the most significant bit (MSB).

C3 to C0 A/D channel number which supplied the data. C3 is the MSB and C0 is the LSB.

BASE + 0 (write) Software A/D triggering

You can trigger an A/D conversion from software, the card's on-board pacer or an external pulse. If you select software triggering, write to the register BASE+0 with any value to trigger an A/D conversion. Bits 1 and 0 of register BASE+9 select the trigger source.

BASE + 1 (write) – A/D range control

Each A/D channel has its own individual input range, controlled by a range code stored in on-board RAM. If you want to change the range code for a given channel, select the channel as the start channel in register BASE+2, MUX scan, then write the range code to bits 0 and 3 of BASE+1.

BASE + 1 A/D range control code (write)								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	N/A	N/A	N/A	N/A	G3	G2	G1	G0

Range codes appear below:

Input range	**Unipolar/bipolar**	**Range code**			
		G3	**G2**	**G1**	**G0**
±5 V	B	0	0	0	0
±2.5 V	B	0	0	0	1
±1.25 V	B	0	0	1	0
±0.625 V	B	0	0	1	1
0 to 10 V	U	0	1	0	0
0 to 5 V	U	0	1	0	1
0 to 2.5 V	U	0	1	1	0
0 to 1.25 V	U	0	1	1	1
±10 V	B	1	0	0	0
N/A		1	0	0	1
N/A		1	0	1	0
N/A		1	0	1	1
N/A		1	1	0	0
N/A		1	1	0	1
N/A		1	1	1	0
N/A		1	1	1	1

BASE + 2 (read/write) MUX scan register

The read/write register at BASE+2 controls multiplexer (MUX) scanning. The high nibble provides the stop scan channel number, and the low nibble provides the start scan channel number. Writing to this register automatically initializes the MUX to the start channel. Each A/D conversion trigger automatically sets the MUX to the next channel.

With continuous triggering the MUX will scan from the start channel to the end channel, then repeat. For example, if the start channel is 3 and the stop channel is 7, then the scan sequence is 3, 4, 5, 6, 7, 3, 4, 5, 6, 7, 3, 4 …

BASE + 2 Start and stop scan channels (write)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	CH3	CH2	CH1	CH0	CL3	CL2	CL1	CL0

CH3 to CH0 Stop scan channel number

CL3 to CL0 Start scan channel number

The MUX scan register low nibble, CL3 to CL0, also acts as a pointer when you program the A/D input range (see BASE+1, above). When you set the MUX start channel to N, the range code written to the register BASE+1 is for channel N.

Programming example

This BASIC code fragment sets the range for channel 5 to ±0.625 V:

```
200  OUT BASE+2, 5    'SET POINTER TO CH.5
210  OUT BASE+1, 3    'RANGE CODE=3 FOR ±0.625 V
```

Note: The MUX start/stop channel changes each time you change the input range. Do not forget to reset the MUX start and stop channels to the correct values after you finish setting the range.

BASE + 3/11 (read/write) Digital I/O registers

The PCL-1800 offers 16 digital input channels and 16 digital output channels. These I/O channels use the input and output ports at addresses BASE+3 and BASE+11.

BASE + 3 D/I low byte (read)								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0

BASE + 3 D/O low byte (write)								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0

BASE + 11 D/I high byte (read)								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8

BASE + 11 D/O high byte (write)								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	DO15	DO14	DO13	DO12	DO11	DO10	DO9	DO8

BASE + 4/5 (write) 8-bit D/A output

The write-only registers BASE+4 and BASE+5 accept data for the PCL-1800's 8-bit D/A output channel (channel 0). The 16-bit register at BASE+26 accepts data for channel 1.

BASE + 4 D/A output low byte (write)								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	DA3	DA2	DA1	DA0	X	X	X	X

BASE + 5 D/A output high byte (write)								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	DA11	DA10	DA9	DA8	DA7	DA6	DA5	DA4

DA11 to DA0 Digital to analog data. DA0 is the least significant bit (LSB) and DA11 is the most significant bit (MSB) of the D/A data.

See also:

BASE+26 – D/A channel 1 data

BASE + 8 (read/write) A/D status register

BASE+8 provides information on PCL-1800's A/D configuration and operation. Writing to this I/O port with any data value clears its INT bit. The other data bits do not change.

BASE + 8 A/D status (read/write)								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	EOC	U/B	MUX	INT	X	X	X	X

EOC End of Conversion.

0 The A/D converter is idle, ready for the next conversion. Data from the previous conversion is available in the A/D data registers.

1 The A/D converter is busy, implying that the A/D conversion is in progress.

U/B Unipolar/bipolar mode indicator

0 Bipolar mode

1 Unipolar mode

MUX Single-ended/differential channel indicator.

0 8 differential channels

1 16 single-ended channels

INT A/D interrupt flag

0 A/D converter busy

1 A/D conversion finished

Remarks

If you trigger the A/D conversion with the on-board pacer or an external pulse, your software should check the INT bit, not the EOC

bit, before it reads the conversion data. EOC can equal 0 in two different situations: the conversion has completed **or** no conversion has been started.

BASE + 9 (read/write) Control register

BASE+9 provides information on the PCL-1800's operating modes.

BASE + 9 Control (read/write)								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	1	0	1	0	X	DMAE1	ST1	ST0

DMAE1 Disable/Enable PCL-1800 DMA transfers.

0 Disables DMA transfer (puts the card in interrupt mode).

1 Enables DMA transfer.

Note: You must program the PC's 8237 DMA controller the DMA page register before you set DMAE to 1.

ST1 to ST0 Trigger source

Trigger source	ST1	ST0
Software trigger	0	X
External trigger	1	0
Pacer trigger	1	1

BASE + 10 (write) Timer/counter enable register

BASE+10 enables or disables the PCL-1800's timer/counter, generally used as a pacer for A/D conversion.

BASE + 10 Enable pacer (write)								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	X	X	X	X	X	X	TC1	TC0

TC0 Disable/enable pacer

0 Pacer enabled

1 Pacer controlled by TRIG0. This setting blocks trigger pulses sent from the pacer to the A/D until TRIG0 is taken high

TC1 Counter 0 input source mode

0 Sets Counter 0 to accept external clock pulses

1 Connects Counter 0 to the PCL-1800's internal 100 KHz clock source

BASE + 12/13/14/15 Programmable timer/counter registers

The four registers located at addresses BASE+12, BASE+13, BASE+14 and BASE+15 access the PCL-1800's Intel 8254 programmable timer/counter. Please refer to Chapter 8 or 8254 product literature for application information.

BASE + 16/17/18 (write) Watchdog comparator

The PCL-1800's 16-channel watchdog comparator ensures fast and reliable response for alarms and triggering conditions. You will need to use the software driver functions to take advantage of this function.

Registers BASE+16 and BASE+17 hold the values to be compared against the analog input. Register BASE+18 holds the watchdog trigger conditions. Before you write the watchdog values for a given channel, you need to set the channel number (BASE+2) and latch it (BASE+25).

To disable watchdog comparator checking for a given level, L1 or L2, on a particular channel set that channel's trigger condition (L1G/L or L2G/L on BASE+18) to 1 and the level test value to FF (hex).

BASE+16, BASE+17 and BASE+18 register formats appear below.

BASE + 16 Test level 1 (tested vs. high byte of A/D data) (write)								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4

AD11 to AD4 Test value. Comparator 1 tests this value against the high byte of the A/D data. DA4 is the least significant bit (LSB) and DA11 is the most significant bit (MSB) of the D/A data

BASE + 17 Test level 2 (tested vs. high byte of A/D data) (write)								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4

AD11 to AD4 Test value. Comparator 2 tests this value against the high byte of the A/D data. DA4 is the least significant bit (LSB) and DA11 is the most significant bit (MSB) of the D/A data

NOTE *Level 1 must be greater than or equal to level 2*

BASE + 18 Watchdog test condition (write)								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	X	X	X	X	L2G/L	1	L1G/L	1

L1G/L The test condition for level 1

1 Sets comparator 1's condition to greater than. If the A/D data > level 1 then comparator 1 activates.

0 Sets comparator 1's condition to less than. If the A/D data < level 1 then comparator 1 activates.

L2G/L The test condition for level 2

1 Sets comparator 2's condition to greater than. If the A/D data > level 2 then comparator 2 activates.

0 Sets comparator 2's condition to less than. If the A/D data < level 2 then comparator 2 activates.

Watchdog trigger condition	**Comparator settings**	
	L1G/L	**L2G/L**
L1 > L2 > data	0	0
Data > L1 > L2	1	1
L1 > data > L2	0	1
Data > L1 or L2 > Data	1	0

To disable watchdog comparator checking for a given level, L1 or L2, on a particular channel set that channel's trigger condition (L1G/L or L2G/L on BASE+18) to 1 and the level test value to FF (hex).

Example

The following BASIC code fragment sets the watchdog for A/D channel 5. The watchdog will trigger if the data is less than 160 (level 1) and greater than 80 (L2).

```
10  OUT BASE+2,5     'Set channel to 5
20  OUT BASE+25,0    'Write any value to latch channel no.
30  OUT BASE+16,160  'Set level 1 to 160
40  OUT BASE+17,80   'Set level 2 to 80
50  OUT BASE+18,13   'Set condition to 0000 1101B
```

BASE + 19 (write) Clear watchdog

Write any value to register BASE+19. This will clear the interrupt generated by the watchdog.

BASE + 21 (read) Status register

The PCL-1800's 1 K word First-In First-Out (FIFO) data buffer stores data from up to 1024 A/D conversions. The FIFO buffer lets you acquire data at up to 330 KHz and prevents data loss under multitasking systems like Windows. See Chapter 5 for more information.

Bit assignments for the FIFO status register appear below:

BASE + 21 Status register (read)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	DMA_TC	CNT_TC	EF	FF	HF	WD_FIG	X	DN_OPEN

EF FIFO empty flag

1 FIFO is empty.

0 FIFO is not empty.

HF FIFO half-full flag

1 FIFO is half-full or more than half-full

0 FIFO is less than half-full

FF FIFO full flag

1 FIFO is full

0 FIFO is not full

DMA_TC DMA flag

1 DMA terminal count

0 No DMA terminal count

CNT_TC Down-counter flag

1 Down-counter has reached zero

0 Down-counter has not yet reached zero

DN_OPEN Down-counter clock open

1 Down-counter can start counting and synchronizing with FIFO

0 Down-counter has stopped counting

BASE + 21 (write) Mode control (FIFO, AD/DA DMA, DMA/INT)

BASE + 21 PCL-1800 mode control (write)								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	N/A	FIFO	AD/DA	DMA/INT	DRQEN	N/A	N/A	N/A

FIFO FIFO select. This setting controls the A/D IRQ request.

0 Allow the A/D IRQ request

1 Disable the A/D IRQ request

AD/DA Select A/D DMA or D/A DMA

0 A/D DMA mode

1 D/A DMA mode

DMA/INT Select DMA or INT mode

0 DMA mode

1 INT mode

DRQEN DMA enable/disable

0 Disable DMA

1 Enable DMA

BASE + 22 (read) Interrupt request source

The PCL-1800 can generate an interrupt request under four different conditions: DMA (A/D or D/A) terminal count (from the PC), FIFO full, watchdog condition met or when the down-counter reaches zero.

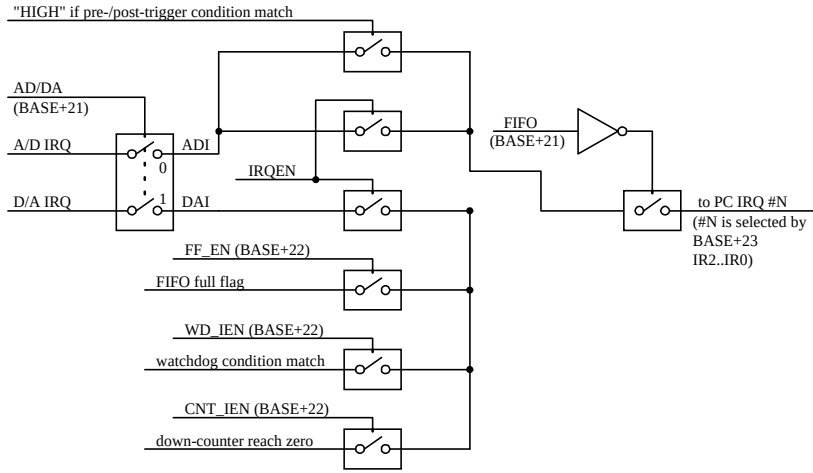
Register level programming for these functions is extremely complicated. You will need to use the card's software driver. See the demo disk and software driver manual for operating instructions.

BASE + 22 Interrupt request source (write)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	IRQEN	DNC_EN	CNT_EN	FE_EN	WD_INT	WDEN	M1	M0

IRQEN Enable/disable the interrupt created by A/D interrupt transfer, A/D DMA and D/A DMA terminal count

CNT_EN	Enable/disable the interrupt produced by the down-counter down counter to zero
FF_EN	Enable/disable the interrupt produced by the FIFO full
M1, M0	Used in pre- and post-trigger modes
DNC_EN	Enable/disable the down-counter function
WDEN	Enable/disable the watchdog function
WD_INT	Enable/disable the interrupt produced by the watchdog comparator



Interrupt circuit tree diagram

BASE + 23 (write)
DMA and interrupt channel selection

The PCL-1800 offers a number of high-performance DMA data transfer options. You can use DMA data transfer for high-speed A/D input or D/A output. You can also use DMA with the card's FIFO buffer and watchdog comparator.

Register level programming for these functions is extremely complicated. You will need to use the card's software driver. See the software driver manual and the demo programs included with the PCL-1800.

The PCL-1800 offers eight interrupt channels: 2, 4, 5, 7, 10, 11, 12, 15. The PCL-1800 driver allows you to select the interrupt channel and enable the required interrupt.

The PCL-1800 also offers three DMA channels: 5, 6 and 7. Dual DMA uses channels 5 and 6.

BASE+23 DMA and interrupt channel selection (write)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	D_DMA	X	DR1	DR0	X	IR2	IR1	IR0

DR1, DR0 Select DMA channel number

DMA channel no.	**DR1**	**DR0**
N/A	0	0
Channel 5	0	1
Channel 6	1	0
Channel 7	1	1

IR0 to IR2 Select interrupt channel number

IRQ no.	**IRQ**	**IR1**	**IR0**
2	0	0	0
4	0	0	1
5	0	1	0
7	0	1	1
10	1	0	0
11	1	0	1
12	1	1	0
15	1	1	1

D-DMA Dual DMA

0 DMA channel is 5, 6 or 7, selected by DR1 and DR0

1 DMA channels are fixed at 5 and 6

BASE + 24 (write)
Time base selection

BASE + 24 Time base selection									
Bit	D7	D6	D5	D4	D3	D2	D1	D0	
Value	Freq	C_mode		X	X	X	X	X	X

Freq Pacer rate

0 Select 1 MHz time base

1 Select 10 MHz time base

C_MODE

User should set C_MODE=1 before the trigger mode changes from internal pacer mode to external mode. Once the change has been made, set the C_MODE=0

NOTE: *User dose not need to change C_MODE when the trigger mode changes from external to internal mode.*

Example:

The following C code extracts changes the trigger mode from internal pacer mode to external mode.

```
outportb (BASE+24,0X40):   /* SET C_MODE=1  */
outportb (BASE+9,0XA6):    /* Enable DMA and external
trigger  */
outportb (BASE+24,0X00):   /* SET C_MODE=0, ready for
                           external TRIGGER SIGNAL  */
```

BASE + 24 (read)
Channel No. which matches watch dog condition

BASE + 24 Time base selection								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	Freq	C_mode		X	X	CH3	CH2	CH1 CH0

CH3 to CH0 Condition matched channel number ranging from channel 0 to channel 15

BASE + 26 (write)
16-bit D/A output

The write-only registers BASE+26 accepts data for the PCL-1800's 16-bit D/A output channel (channel 1). The 8-bit registers at BASE+4 and BASE+5 accepts data for channel 0.

BASE + 26 D/A output Channel 1, 16-bit								
Bit	D15	D14	D13	D12	D11	D10	D9	D8
Value	X	X	X	X	DA11	DA10	DA9	DA8
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

DA15 to DA0 Digital to analog data. DA0 is the least significant bit (LSB) and DA15 is the most significant bit (MSB) of the D/A data.

See also:

BASE+4/5 – D/A channel 0 data

BASE + 28/29 (write) Down-counter

PCL-1800 provides a down-counter with an 11-bit auto-reload function. We designed the down-counter especially to control the data in the FIFO.

You will need to use the software driver for this function. See Chapter 5 for operating instructions.

Register format is as follows:

BASE + 28 Down counter value, low byte (write)								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	C7	C6	C5	C4	C3	C2	C1	C0

BASE + 29 Down counter value, high three bits (write)								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	X	X	X	X	X	C10	C9	C8

C10 to C0 The down-counter value

***Note**: Read BASE+28 to clear the down-counter flag (BASE+21 bit 6)*

BASE + 30 (read) Card ID code

You can read the PCL-1800's ID code at register BASE+30. The first time you read this register, it will return 00 (hex). The second time you read it, it will return 18 (hex). Your program can use this ID code to identify the PCL-1800 and automatically search for the location of the card's base address.

CHAPTER 5

A/D conversion

This chapter explains how to use the PCL-1800's A/D conversion functions. The PCL-1800 gives you a wide array of options for triggering and data transfer.

You can trigger the data conversions from software, the card's on-board pacer or an external signal.

You can transfer the acquired data using software, interrupt or DMA. In addition, you can use the card's FIFO buffer to store the data then transfer it through any of the above methods except DMA.

A/D data format and status register

A 16-bit read-only register at BASE+0 holds data from each A/D conversion and identifies the source A/D channel number. Bits D15 (the MSB) to D4 (the LSB) hold the 12 bits of data from the conversion. Bits D3 (the MSB) to D0 (the LSB) hold the source A/D channel number.

BASE+0	A/D conversion data and channel number (read only)							
Bit	D15	D14	D13	D12	D11	D10	D9	D8
Value	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	AD3	AD2	AD1	AD0	C3	C2	C1	C0

AD11 to AD0 Analog to digital conversion data. AD0 is the least significant bit (LSB) of the A/D data, and AD11 is the most significant bit (MSB).

C3 to C0 A/D channel number which supplied the data. C3 is the MSB and C0 is the LSB.

If you select software triggering, discussed below, write to BASE+0 with any value to trigger an A/D conversion.

A/D status register – BASE + 8

The read-only register at BASE+8 holds configuration and status information, including:

- Bipolar or unipolar input for the channel to be converted next
- Single-ended or differential input
- Interrupt status for the channel already converted
- End of conversion for the channel already converted
- Channel to be converted next

Refer to Chapter 4, *A/D status register* for more information.

The format for the A/D status register is:

BASE + 8 A/D status (read/write)								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	EOC	U/B	MUX	INT	X	X	X	X

EOC End of Conversion.

0 The A/D converter is idle, ready for the next conversion. Data from the previous conversion is available in the A/D data registers.

1 The A/D converter is busy, implying that the A/D conversion is in progress.

U/B Unipolar/bipolar mode indicator

0 Bipolar mode

1 Unipolar mode

MUX Single-ended/differential channel indicator.

0 8 differential channels

1 16 single-ended channels

INT A/D interrupt flag

0 A/D converter busy

1 A/D conversion finished

Remarks

If you trigger the A/D conversion with the on-board pacer or an external pulse, your software should check the INT bit, not the EOC bit, before it reads the conversion data.

EOC can equal 0 in two different situations: the conversion has completed **or** no conversion has been started.

Input range, MUX and trigger settings

Before the A/D conversion operation you will need to set the input range for each channel and the channel range to be scanned by the MUX (multiplexer). You will also need to set up the trigger source for the conversion. You can program each of these settings in software.

Input range selection

Each A/D channel has its own individual input range, controlled by a range code stored in on-board RAM. If you want to change the range code for a given channel, select the channel as the start channel in register BASE+2, MUX scan, then write the range code to bits D0 and D1 of BASE+1.

BASE+1 A/D range control code (write)								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	N/A	N/A	N/A	N/A	G3	G2	G1	G0

Range codes appear below:

Input range	Unipolar/bipolar	Range code			
		G3	G2	G1	G0
±5 V	B	0	0	0	0
±2.5 V	B	0	0	0	1
±1.25 V	B	0	0	1	0
±0.625 V	B	0	0	1	1
0 to 10 V	U	0	1	0	0
0 to 5 V	U	0	1	0	1
0 to 2.5 V	U	0	1	1	0
0 to 1.25 V	U	0	1	1	1
±10 V	B	1	0	0	0
N/A		1	0	0	1
N/A		1	0	1	0
N/A		1	0	1	1
N/A		1	1	0	0
N/A		1	1	0	1
N/A		1	1	1	0
N/A		1	1	1	1

MUX setting

The PCL-1800 offers 16 single-ended or eight differential analog input channels. Set switch SW1 for the channel configuration before you set the multiplexer scan range. The MUX scan register, address BASE+2, specifies the high and low limits of the scan range. Bits D0 to D3 hold the starting channel number, and positions D4 to D7 hold the end scan channel number. When you set the PCL-1800 for eight differential input channels, you must set bits CH3 and CL3 to zero.

The MUX scan register data format is:

BASE+2 start and stop scan channels (write)								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	CH3	CH2	CH1	CH0	CL3	CL2	CL1	CL0

If you require only one A/D input channel, you should set the high and low scan limits to the same value. If you specify a range of input channels, the PCL-1800 automatically performs an A/D conversion on each channel in the range, beginning with the start channel. When it reaches the end channel, it loops back to the start channel and continues. This looping continues until the specified number of conversions is completed. Note that the MUX channel is automatically reset to the start channel whenever you write to it.

You can specify channel settings by writing directly to the MUX scan register. You use the MUX scan register to point to a specified channel when you set channel input ranges (with BASE+1). After you set the input range, you will need to reset the MUX register for the proper start and stop channels.

Trigger mode

You can trigger an A/D conversion from software, the card's on-board pacer or an external pulse (CN3, pin 35). Select the trigger source by programming bits D0 and D1 of register BASE+9.

Software

If you select software triggering, write to register BASE+0 with any value to trigger the A/D conversion. You would not use software triggering in high speed A/D applications because the triggering rate is too slow.

On-board pacer

You can use the PCL-1800's on-board Intel 8254 programmable interval timer/counter to generate timing related signals. Counters 1 and 2 of the Intel 8254 can provide A/D converter trigger pulses with precise periods. The 8254 can generate pacer output between 2.5 MHz and 71 minutes per pulse. Chapter 8 covers the details of the Intel 8254 timer/counter.

Pacer triggering is ideal for interrupt and DMA data transfer, normally used in A/D applications which require higher conversion speeds.

External trigger

You can provide an external signal to trigger the A/D conversion. Connect the external signal to A/D EXT. TRIG (pin 35 on connector CN3). You would normally use external triggering if your application requires A/D conversions conditionally, not periodically, e.g., measuring a voltage when a limit switch closes. The A/D conversion starts at the rising edge of the external trigger pulse.

A/D data transfer

The PCL-1800 can transfer A/D data by program control, interrupt routine or DMA.

You can transfer the data from each conversion to the PC immediately, or you can store data from a series of conversions in the FIFO (First In First Out) buffer and copy it all at once.

In addition, you can use the PCL-1800's watchdog comparator circuit to transfer the collected data only when it meets specific conditions.

Program- and interrupt-controlled data transfer are straightforward. DMA data transfer, however, can be quite complicated, because the PCL-1800 uses dual-buffer 16-bit DMA. Unless you are extremely experienced with the PC and PCL-1800 (and have a high tolerance for pain) we recommend that you use the PCL-1800 software driver.

Program-controlled data transfer (without FIFO)

In program controlled data transfer your program polls the card to see when the card has finished an A/D conversion, then accesses the data by reading it from the card's I/O port (BASE+0).

If you use software triggering, your program should trigger an A/D conversion (by writing any value to BASE+0), then poll the EOC (end of conversion) bit in the A/D status register (BASE+8). When EOC is off, the converter has finished processing the data. Your program can then read the data from the A/D data registers.

If you use pacer or externally triggered A/D, your application program should check the EOC bit (end of conversion) of the A/D status register (BASE+8). If this bit is off (0), an A/D conversion is in progress. When the EOC bit is on, the conversion is finished and the data has been placed in the A/D data register (BASE+0). Your program can then read the data.

You can also use the PCL-1800's FIFO buffer to store the data, as described in the following section.

Interrupt-routine data transfer

With interrupt routine data transfer, you write an interrupt service routine (ISR) program to transfer data from the card's A/D data registers to a previously defined memory segment in the PC. At the end of each conversion the EOC signal generates an interrupt, and the ISR performs the transfer. You will need to specify the interrupt control bit and the interrupt level selection bits in the PCL-1800 control registers (BASE+21, 22 and 23) before you use the interrupt routine. Writing to the A/D status register address (BASE+8) resets and re-enables the PCL-1800's A/D interrupt request.

You can use the PCL-1800's FIFO buffer, described below, to protect against data loss.

DMA transfer

Direct memory access (DMA) transfer moves the A/D data from the PCL-1800 hardware to the PC system memory without the system CPU. The PCL-1800 offers 16-bit single and dual DMA. Dual DMA lets you continue collecting or outputting data during the DMA data transfer, however, the DMA channels cannot be configured for A/D and D/A at the same time. Register-level programming is extremely complex; we strongly recommend that you use the PCL-1800's software driver.

With single-channel DMA you can software select DMA channels 5, 6 or 7. Dual DMA is limited to DMA channels 5 and 6.

Dual DMA uses two data buffers and two DMA channels (channels 5 and 6). The card first DMA channel 5 to copy data to the first buffer. When this buffer becomes full, the card automatically starts copying

data to the second buffer through channel 6. Your program can then remove the data from the first buffer.

When the second buffer becomes full, the card switches back to the first buffer. Your program can then transfer the data from the second buffer.

When you set the card's level trigger to position-trigger mode (BASE+22, M1, M0 = 11), the watchdog comparator will switch DMA transfer between DMA channels 5 and 6.

Otherwise, the TC (DMA terminal count) signal will switch the DMA transfer between DMA channels 5 and 6 in dual-DMA mode.

FIFO

General information

The PCL-1800's FIFO (First In First Out) buffer It lets you acquire data at up to 330 KHz and protects you from data loss with high data rates, especially under multitasking operating systems like Windows.

Normally, the PCL-1800 transfers data from A/D conversions one element at a time. It performs a conversion, writes the data to the data output register, then transfers the data using DMA or an interrupt service routine.

Without the FIFO, the each time the card performs a conversion, the data overwrites existing data in the output register. If the old data is not removed before the new data arrives, the old data is lost.

With the FIFO enabled (BASE+21, bit 6 = 1) the new data simply fills the second element in the buffer, leaving the original data intact. Data from each further conversion fills the other elements in the FIFO. The FIFO holds data from up to 1024 conversions.

When you want to remove data from the FIFO, simple read a data element from the data register (BASE+0). This pulls the earliest data from the FIFO; the next data element in the FIFO takes its place. You can transfer data elements from the FIFO buffer at any time. The card continues saving data to the FIFO even as you are removing the old data, preventing data loss.

You can also wait until the FIFO becomes full or half full, then remove all the elements at once. This method allows extremely fast data transfer, because it minimizes the number of instructions the CPU must perform. The RIS (repeat input string) command in the 80x86 instruction set allows you to repeatedly transfer data elements with one command.

Software-controlled data transfer

Programming with the FIFO is similar to standard software-controlled data transfer. Three flags in BASE+21 indicate the status of the FIFO: the empty flag (EF), half-full flag (HF) and full-flag (FF). If you want to remove data as the card acquires it, poll EF. If EF is 0, one or more conversions have occurred and data is available in the FIFO. Your program should then read each element in turn from BASE+0, checking EF to determine when the FIFO is empty.

You can also wait for the FIFO to become full or half full before you empty it. Simply poll the HF or FF flag.

Interrupt-controlled data transfer

The PCL-1800's FIFO buffer can protect you from data loss. In normal operation, the PCL-1800 generates an interrupt when it has finished converting the A/D data, and your interrupt service routine (ISR) transfers the data. A problem occurs, however, when a higher-priority system interrupt blocks the PCL-1800's interrupt. Your ISR must wait until the system interrupt has finished before it can transfer the data. If the wait is too long, the PCL-1800 may perform another A/D conversion and overwrite the data in the A/D data registers before your routine can transfer the old data. The new A/D conversion will call your ISR again, but it will only transfer the new data.

The PCL-1800's FIFO buffer solves this problem. The FIFO stores the data elements from each successive A/D conversion. If your ISR cannot transfer the first element in the buffer before the next conversion, the FIFO simply stores the data from the second conversion at the next position.

The programming procedure with the FIFO is basically the same as with the standard data registers. The only difference is that your ISR should transfer as many data elements as are in the FIFO buffer, not just a single element. It should read an element from the data register (BASE+0) then check the FIFO empty flag, bit 5 of BASE+21. When bit 5 is 1, the buffer is empty.

Using the down-counter

The PCL-1800's down counter lets you control how many data elements are in the FIFO. Simply set the down counter for the number of elements you want to store before transferring data to the PC. Each time the card stores a data element in the FIFO, it decrements the down counter. When the down counter reaches zero, it sets the down-counter-empty flag or generates an interrupt (set by BASE+22).

Flushing the FIFO

If you want to flush the FIFO buffer, write any value to BASE+30. This will empty the FIFO and set the empty flag (bit 5 of BASE+21) to 1. The half-full flag (bit 4) and full flag (bit 5) will be set to 0.

Watchdog comparator

Two 8-bit comparators on each input line store test values and compare the values against the reading on the input line. Each comparator tests its 8-bits against the highest eight bits of the 12-bit A/D conversion data. If the A/D data meets the preset conditions, the watchdog circuit generates an interrupt or sets flags (bits 2 and 3 of BASE+22).

This control logic lets you set up complex alarming and triggering conditions. For example, you can set the watchdog to trigger if the input is above the high-level value or below the low-level value.

See Chapter 4 for more information.

Down-counter

The PCL-1800's down counter lets you acquire a specific number of A/C conversions in the FIFO buffer, then transfer them by software or interrupt.

Each time the PCL-1800 stores data from an A/D conversion in the FIFO, the card reduces the value in the down-counter by one. When the value in the down-counter reaches zero, the PCL-1800 sets the down-counter-terminal-count flag, CNTTC, (sets BASE+22 bit 6 to 1) or generates an interrupt (sets BASE+22 bit 5 to 1). The PCL-1800 then reloads the down counter with the initial value and starts counting down again with the next A/D conversion.

You can then copy the data to the PC. You have two choices: your program can poll the CNTTC flag and copy the data when it is 1, or you can write an interrupt service routine to copy the data.

In either case, after you transfer the data you should reset the CNTTC flag by reading BASE+28.

Synchronizing the down-counter and FIFO

The DN_OPEN flag (BASE+21 bit 0) serves as a gate to control whether the down-counter counts down when data arrives in the FIFO. When the DN_OPEN flag is 1, the down-counter counts down when the A/D converter writes the data to the FIFO. When the flag is 0, the down-counter does not count down.

You would usually use the DN_OPEN flag to synchronize the down-counter so that it counts the number of elements in the FIFO buffer.

Before you reset the FIFO (by writing to BASE+30), set DN_OPEN to 0. When you reset the FIFO, DN_OPEN will automatically be toggled to 1.

Setting the initial value

Register BASE+28 stores bits 0 to 7 of the down-counter value, and register BASE+29 stores bits 8 to 10.

Reset the down counter (change bit 7 of BASE+22 to 0 then back to 1). You can then load the initial value directly into the down-counter. Write the starting value low byte to register BASE+28, then write the high byte to register BASE+29.

When the down counter is counting, the PCL-1800 latches any data you write to registers BASE+28 and BASE+29 in a buffer. When the down-counter reaches zero, the PCL-1800 automatically loads the buffer values into the down counter.

Disabling the down-counter

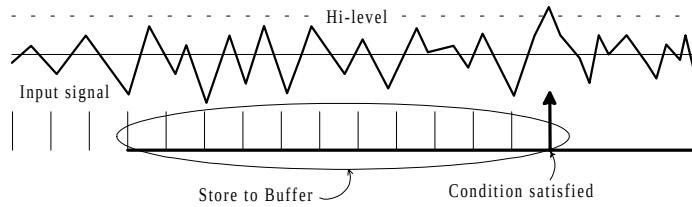
You can disable the down counter by loading a zero as the initial value or by setting BASE+22 bit 7 to 0 (the default).

Level-triggering

The PCL-1800's level triggering function, along with the watchdog comparator, acts as a gate controlling the flow of A/D data to the PC. The level trigger has three modes: pre-trigger, post-trigger and position-trigger.

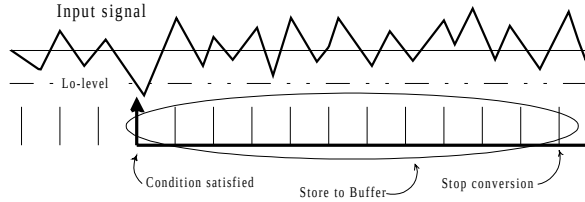
Pre-trigger mode

In pre-trigger mode the PCL-1800 acquires data normally and sends it to the PC. When the data satisfies the conditions of the watchdog comparator, the card stops acquiring data and generates an interrupt (or simply sets a flag).



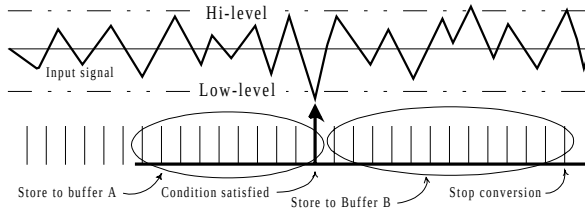
Post-trigger mode

In post-trigger mode the PCL-1800 converts analog input data and the watchdog comparator checks it. When the data satisfies the conditions of the watchdog comparator, the card begins sending data to the PC.



Position-trigger mode

In position-trigger mode the PCL-1800 converts a user-specified number of analog input data readings and sends them to buffer A in the PC. After the input data satisfies the conditions of the watchdog comparator, the card begins sending the data to buffer B in the PC. It sends a user-specified number of data elements to buffer B, then stops.



Operation

Pre- and post-trigger modes support standard DMA, interrupt and software controlled data transfer. Position-trigger mode only works with DMA data transfer.

You select the mode as follows:

Pre-trigger mode	BASE+22 M1=0, M0=1
Post-trigger mode	BASE+22 M1=1, M0=0
Position-trigger mode	BASE+22 M1=1, M0=1 BASE+23 D_DMA=1

CHAPTER 6

D/A conversion

General information

The PCL-1800 provides two 12-bit D/A output channels, channel 0 and channel 1. Channel 1 supports 16-bit DMA (direct memory access) data transfer. Channel 1 can output D/A data from your PC at up to 200 KHz. This lets you use the PCL-1800 as a programmable function generator. A/D channel 1 also supports dual DMA. You can use two data buffers to create more waveforms, and you can trigger the D/A conversion from software, the card's on-board pacer or an external pulse (CN3, pin 16).

The PCL-1800 provides a precision fixed internal -5 V or -10 V reference, selectable by means of Jumper JP3. This reference voltage is available at connector CN3 pin 11. If you use this voltage as the D/A reference input, the D/A output range is either 0 to +5 V or 0 to +10 V. You can also use an external DC or AC source as the D/A reference input. In this case, the maximum reference input voltage is ±10 V, and the maximum D/A output ranges are 0 to +10 V or 0 to -10 V.

Connector CN3 supports all D/A signal connections. Chapter 2 gives connector pin assignments. Chapter 3 gives a wiring diagram for D/A signal connections.

Channel 0 – 8-bit data transfer

Write registers at addresses BASE+4 and BASE+5 hold output data for channel 0. DA0 is the least significant bit (LSB) and DA11 is the most significant bit (MSB) of the D/A data. The register data format appears below:

BASE+4 D/A output channel 0, 8-bit (low byte)								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	DA3	DA2	DA1	DA0	X	X	X	X

BASE+5 D/A output Channel 0, 8 bit (high byte)								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	DA11	DA10	DA9	DA8	DA7	DA6	DA5	DA4

When you write data to the D/A channel 0, write the low byte first. The low byte is temporarily held by a register in the D/A and not released to the output. After you write the high byte, the low byte and high byte are added and passed to the D/A converter. This double buffering process protects the D/A data integrity through a single step update.

Channel 1 – 16-bit data transfer

The write register at BASE+26 holds output data for channel 1. DA0 is the least significant bit (LSB) and DA11 is the most significant bit (MSB) of the D/A data. The register data format appears below:

BASE+26 D/A output Channel 1, 16-bit								
Bit	D15	D14	D13	D12	D11	D10	D9	D8
Value	X	X	X	X	DA11	DA10	DA9	DA8
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

D/A applications

The PCL-1800 supports a variety of D/A operations. It can, for example, function as a digital attenuator (by inputting variable AC or DC references) or as a generator of arbitrary waveforms.

In your application program you can perform D/A functions by addressing the PCL-1800's registers directly, or you can take advantage of the Advantech driver functions. See the user's manual for the driver for more information.

CHAPTER 7

Digital input and output

The PCL-1800 provides 16 digital input channels and 16 digital output channels. The registers at addresses BASE+3 and BASE+11 hold input and output data. Data format for each register appears below:

BASE + 3 D/I low byte (read)								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0

BASE + 3 D/O low byte (write)								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0

BASE + 11 D/I high byte (read)								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8

BASE + 11 D/O high byte (write)								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	DO15	DO14	DO13	DO12	DO11	DO10	DO9	DO8

Using the PCL-1800's input and output functions is fairly straightforward. Chapter 3 gives some ideas for digital signal connections.

CHAPTER 8

Programmable timer/counter

The Intel 8254

The PCL-1800 uses the Intel 8254 programmable interval timer/counter. The popular 8254 offers three independent 16-bit down counters. Each counter has a clock input, control gate and an output. You can program each counter for maximum count values from 2 to 65535.

The 8254 has a maximum input clock frequency of 10 MHz. The PCL-1800 provides 1 MHz and 10 MHz input frequencies to the 8254 from an on-board crystal oscillator. You can set the clock input frequency in software (BASE+24 bit 7). See Chapter 4 for more information.

The PCL-1800 cascades Counters 1 and 2 on the 8254 and operates them in a fixed divider configuration. Counter 1 input connects to the 1 MHz or 10 MHz clock frequency. The output of Counter 1 connects to the input of Counter 2. The output of Counter 2 is internally configured to provide trigger pulses to the A/D converter, but you can also access it for your own use through connector CN3 pin 37. The PCL-1800 does not use Counter 0, so you can use it for your applications. You access Counter 0 through CN3 pin 18.

Counter read/write and control registers

The 8254 programmable interval timer uses four registers at addresses BASE+12, BASE+13, BASE+14 and BASE+15. Register functions appear below:

Register	Function
BASE+12	Counter 0 read/write
BASE+13	Counter 1 read/write
BASE+14	Counter 2 read/write
BASE+15	Counter control word

Since the 8254 counter uses a 16-bit structure, each section of read/write data is split into a least significant byte (LSB) and most significant byte (MSB). To avoid errors it is important that you make read/write operations in pairs and keep track of the byte order.

The data format for the control register appears below:

BASE + 15 8254 control, standard mode								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC1 & SC0 Select counter.

Counter	SC1	SC0
0	0	0
1	0	1
2	1	0
Read-back command	1	1

RW1 & RW0 Select read/write operation

Operation	RW1	RW0
Counter latch	0	0
Read/write LSB	0	1
Read/write MSB	1	0
Read/write LSB first, then MSB	1	1

M2, M1 & M0 Select operating mode

M2	M1	M0	Mode	
0	0	0	0	programmable one shot
0	0	1	1	programmable one shot
X	1	0	2	Rate generator
X	1	1	3	Square wave rate generator
1	0	0	4	Software triggered strobe
1	0	1	5	Hardware triggered strobe

BCD Select binary or BCD counting.

BCD	Type
0	Binary counting 16-bits
1	Binary coded decimal (BCD) counting

If you set the module for binary counting, the count can be any number from 0 up to 65535. If you set it for BCD (Binary Coded Decimal) counting, the count can be any number from 0 to 9999.

If you set both SC1 and SC0 bits to 1, the counter control register is in read-back command mode. The control register data format then becomes:

BASE+15	8254 control, read-back mode							
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	1	1	CNT	STA	C2	C1	C0	X

CNT = 0 Latch count of selected counter(s).

STA = 0 Latch status of selected counter(s).

C2, C1 & C0 Select counter for a read-back operation.

C2 = 1 select Counter 2

C1 = 1 select Counter 1

C0 = 1 select Counter 0

If you set both SC1 and SC0 to 1 and STA to 0, the register selected by C2 to C0 contains a byte which shows the status of the counter. The data format of the counter read/write register then becomes:

BASE + 12/13/14	Status read-back mode							
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	OUT	NC	RW1	RW0	M2	M1	M0	BCD

OUT Current state of counter output

NC Null count is 1 when the last count written to the counter register has been loaded into the counting element

The counter enable register, located at address BASE+10, has a close relationship with the counter operation. Refer to Chapter 4, *Timer/ counter enable register,* for the register data format. The TC0 bit enables and disables the pacer. If TC0 = 0, the pacer is disabled. If TC0 = 1, the pacer is disabled and trigger pulses from the pacer are kept from the A/D until TRIG0 is taken high. The TC1 bit controls the input source for Counter 0. If TC1 = 0, Counter 0 is configured to accept external clock pulses. If TC1 = 1, Counter 0 is internally connected to the 100 KHz clock source.

Counter operating modes

MODE 0 – Stop on terminal count

The output will be initially low after you set this mode of operation. After you load the count into the selected count register, the output will remain low and the counter will count. When the counter reaches the terminal count, its output will go high and remain high until you reload it with the mode or a new count value. The counter continues to decrement after it reaches the terminal count. Rewriting a counter register during counting has the following results:

1. Writing to the first byte stops the current counting.
2. Writing to the second byte starts the new count.

MODE 1 – Programmable one-shot

The output is initially high. The output will go low on the count following the rising edge of the gate input. It will then go high on the terminal count. If you load a new count value while the output is low, the new value will not affect the duration of the one-shot pulse until the succeeding trigger. You can read the current count at any time without affecting the one-shot pulse. The one-shot is retriggerable, thus the output will remain low for the full count after any rising edge at the gate input.

MODE 2 – Rate generator

The output will be low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the counter register. If you reload the counter register between output pulses, the present period will not be affected, but the subsequent period will reflect the value.

The gate input, when low, will force the output high. When the gate input goes high, the counter will start from the initial count. You can thus use the gate input to synchronize the counter.

With this mode the output will remain high until you load the count register is loaded. You can also synchronize the output by software.

MODE 3 – Square wave generator

This mode is similar to Mode 2, except that the output will remain high until one half of the count has been completed (for even numbers), and will go low for the other half of the count. This is accomplished by decreasing the counter by two on the falling edge of each clock pulse. When the counter reaches the terminal count, the state of the output is changed, the counter is reloaded with the full count and the whole process is repeated.

If the count is odd and the output is high, the first clock pulse (after the count is loaded) decrements the count by 1. Subsequent clock pulses decrement the count by 2. After timeout, the output goes low and the full count is reloaded. The first clock pulse (following the reload) decrements the counter by 3. Subsequent clock pulses decrement the count by two until timeout, then the whole process is repeated. In this way, if the count is odd, the output will be high for (N+1)/2 counts and low for (N-1)/2 counts.

MODE 4 – software triggered strobe

After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one input clock period then go high again.

If you reload the count register during counting, the new count will be loaded on the next CLK pulse. The count will be inhibited while the GATE input is low.

MODE 5 – Hardware triggered strobe

The counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable.

Counter operations

Read/write operation

Before you write the initial count to each counter, you must first specify the read/write operation type, operating mode and counter type in the control byte and write the control byte to the control register (BASE+15).

Since the control byte register and all three counter read/write registers have separate addresses and each control byte specifies the counter it applies to (by SC1 and SC0), no instructions on the operating sequence are required. Any programming sequence following the 8254 convention is acceptable.

There are three types of counter operation: read/load LSB, read /load MSB and read /load LSB followed by MSB. It is important that you make your read/write operations in pairs and keep track of the byte order.

Counter read-back command

The 8254 counter read-back command lets you check the count value, programmed mode and current states of the OUT pin and Null Count flag of the selected counter(s). You write this command to the control word register. Format is as shown at the beginning of the chapter.

The read-back command can latch multiple counter output latches. Simply set the CNT bit to 0 and select the desired counter(s). This single command is functionally equivalent to multiple counter latch commands, one for each counter latched.

The read-back command can also latch status information for selected counter(s) by setting STA bit = 0. The status must be latched to be read; the status of a counter is accessed by a read from that counter. The counter status format appears at the beginning of the chapter.

Counter latch operation

Users often want to read the value of a counter without disturbing the count in progress. You do this by latching the count value for the specific counter then reading the value.

The 8254 supports the counter latch operation in two ways. The first way is to set bits RW1 and RW0 to 0. This latches the count of the selected counter in a 16-bit hold register. The second way is to perform a latch operation under the read-back command. Set bits SC1 and SC0 to 1 and CNT = 0. The second method has the advantage of operating several counters at the same time. A subsequent read operation on the selected counter will retrieve the latched value.

Counter applications

The 8254 programmable interval timer/counter on your PCL-1800 interface card is a very useful device. You can program counters 1 and 2 to serve as a pacer to generate A/D conversion trigger pulses. Counter 0 is not committed to any internal use. You can configure it for any supported function, e.g., a square wave generator.

CHAPTER 9

Direct memory access operation

Direct memory access (DMA) allows external devices to transfer information directly to or from the PC's memory without the system CPU. The PCL-1800's DMA capability offers high speed transfer. However, the fastest transfer comes when you use the card's FIFO buffer.

Introduction to the 8237 DMA controller

8237 DMA controller chips on the PC system board handle DMA operations. The PC normally has two 8237 chips, one master and one slave.

Each 8237 chip has four DMA transfer channels. Channels 0 to 3 are on the slave chip. Channels 4 to 7 are on the master chip. Channel 4 cascades from the master chip. Channels 0 to 3 are 8-bit access, channels 5 to 7 are 16-bit access. The PCL-1800 uses channels 5, 6 and 7 on the master chip.

Each channel has two associated control signals associated with it. The DMA request signal (DRQ) triggers a DMA operation, and the DMA acknowledge signal (DACK) authorizes the 8237 to start the data transfer.

The 8237 DMA chip has four control registers. These registers are:

1. Operation mode register (sets the mode of operation, in this case single mode)
2. Address register (specifies the memory segment starting address)
3. Word count register (specifies the number of transfers)
4. Initialization register (enables DMA channels)

You must properly set all four registers before you request the DMA operation.

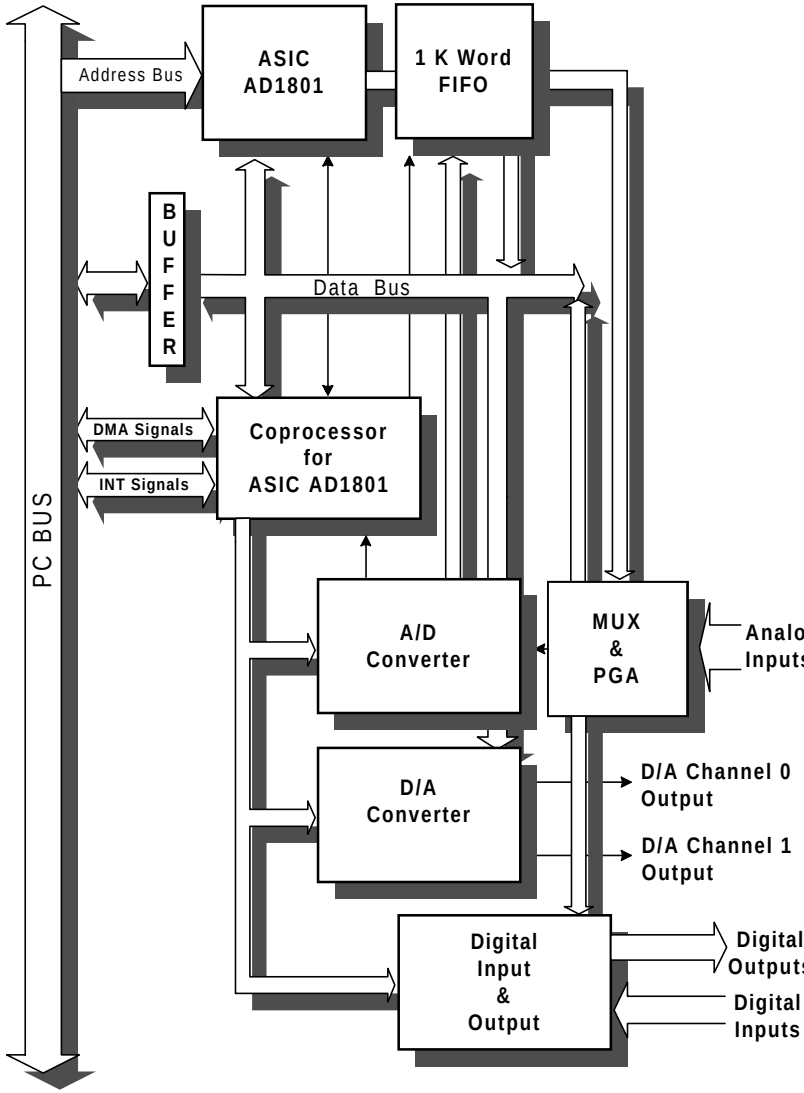
Using DMA transfer with the PCL-1800

DMA transfer is a powerful but complicated operation. Chapter 5 covers A/D conversion with DMA data transfer, and Chapter 6 covers D/A with DMA data transfer. The following steps summarize how to use DMA transfer with the PCL-1800:

1. If you will be using the PCL-1800 driver for your DMA transfer programming, see the Software Drivers User's Manual for information.
2. If you choose to conduct your own DMA operation, you will need to have a solid understanding of the PC, 8237 DMA controller and the PCL-1800. Make sure you perform the following steps in your DMA transfer:
   a. Initialize the 8237's DMA controller register and page register.
   b. Select the DMA channel used by the PCL-1800 (BASE+23 DR1 and DR0).
   c. Select DMA and enable the card's DMA request (BASE+21 DMA/INT = 0 and DRQEN=1).
   d. Set up an external trigger pulse or pacer trigger rate.
   e. Clear the PC DMA channel mask
   f. Enable the trigger source to start the A/D conversion

APPENDIX A

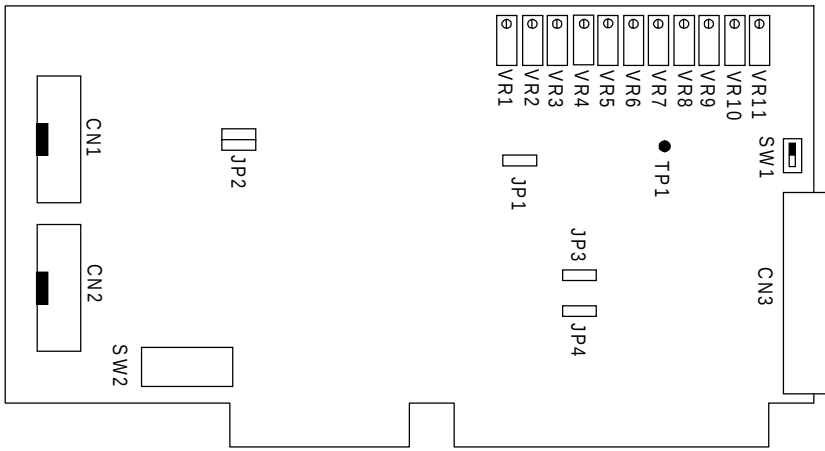
Block Diagram



PCL-1800 block diagram

APPENDIX B

Connector, switch and VR Locations



Card connectors, switches and VR locations

Part	Function	Part	Function
VR1	A/D bipolar offset	**CN1**	Digital output
VR2	A/D unipolar offset	**CN2**	Digital input
VR3	D/A full scale	**CN3**	Analog input/analog output
VR4	A/D full scale	**SW1**	Differential/single-ended input
VR5	PGA out offset	**SW2**	Base address
VR6	D/A 0 offset	**JP1**	-5 V/-10 V reference
VR7	D/A 1 offset	**JP2**	TRIG0, GATE0 connection
VR8	PGA gain = 1 offset	**JP3**	D/A 0 reference selection
VR9	PGA gain = 2 offset	**JP4**	D/A 1 reference selection
VR10	PGA gain = 4 offset		
VR11	PGA gain = 8 offset		
TP1	Test point		

APPENDIX C

PC I/O port address map

PC I/O port address map

Range (hex)	Function
000 - 1FF	Base system
200	Reserved
201	Game control
202 - 277	Reserved
278 - 27F	LPT2: (2nd printer port)
280 - 2F7	Reserved
2F8 - 2FF	COM2:
300 - 377	Reserved
378 - 37F	LPT1: (1st printer port)
380 - 3AF	Reserved
3B0 - 3BF	Mono Display/Print adapter
3C0 - 3CF	Reserved
3D0 - 3DF	Color/Graphics
3E0 - 3EF	Reserved
3F0 - 3F7	Floppy disk drive
3F8 - 3FF	COM1:

APPENDIX D

Calibration

Regular calibration checks are ensure accuracy in data acquisition and control applications. We provide a calibration program, CALB1800.EXE, on the PCL-1800 software disk to assist you.

The minimum equipment you will need for a satisfactory calibration is a 4½-digit digital multimeter and a voltage calibrator or stable, noise free D. C. voltage source. You may also want a card extender, such as the Advantech PCL-757 ISA-Bus Switch/Extension Card. The PCL-757 transparently extends the PC-bus connector to the top of the chassis, giving safe and easy access to the PCL-1800 during calibration or other tasks.

The CALB1800.EXE program included with your card makes calibration easy. It leads you through the calibration and setup procedure with a variety of prompts and graphic displays, showing you all of the correct settings and adjustments. The explanatory material in this section is brief and is intended for use in conjunction with the calibration program.

VR assignment

The 11 variable resistors (VRs) on the PCL-1800 board help you make accurate adjustments on all A/D and D/A channels. See the figure in Appendix B for help finding the VRs. The following list shows the function of each VR:

VR	Function
VR1	A/D bipolar offset
VR2	A/D unipolar offset
VR3	D/A full scale (DA V_{ref})
VR4	A/D full scale
VR5	PGA out offset
VR6	D/A 0 offset
VR7	D/A 1 offset
VR8	PGA gain = 1 offset
VR9	PGA gain = 2 offset
VR10	PGA gain = 4 offset
VR11	PGA gain = 8 offset

A/D calibration

Regular and accurate calibration ensures maximum possible accuracy. The CALB1800.EXE calibration program leads you through the whole A/D offset and gain adjustment procedure. The basic steps appear below:

1. Power on the PCL-1800 for at least 10 minutes to warm up the PGA.
2. Short the A/D input channel 0 to ground.
3. Set the PCL-1800 gain to 2. Measure the voltage at TP1 on the PCB (see the figure in Appendix B). Adjust VR5 until TP1 is as close as possible to 0 V.
4. Set gain codes (1, 2, 4 and 8) and adjust the corresponding variable resistors (VR8, 9, 10 and 11) for each to set TP1 as close as possible to 0 V.
5. Repeat step 4, adjusting the output for each gain code again.
6. Select bipolar input configuration. Connect a DC voltage source with value equal to 0.5 LSB (such as the D/A output) to A/D Channel 0 (pin 1 on connector CN3).
7. Adjust VR1 until the A/D reading flickers between 2048 and 2049.
8. Connect a DC voltage source with a value of 4094.5 LSB (such as the D/A output) to A/D channel 0.
9. Adjust VR4 until the A/D reading flickers between 4094 and 4095.
10. Repeat steps 6 to 9 to adjust the bipolar offset (VR1) and A/D full scale (VR4).
11. Select unipolar input configuration. Connect a DC voltage source with a value of 0.5 LSB (such as the D/A output) to A/D channel 0. Adjust VR2 until the reading of the A/D flickers between 0 and 1.

D/A calibration

You can use either the on-board -5 V (-10 V) reference or an external reference (within the range ±10 V) to calibrate the D/A output.

1. If you use an external reference, set jumper JP3 (ch. 0) or JP4 (ch. 1) to EXT. Connect the external reference to Pin 11 of CN3, V.REF.

   If you are using internal reference, adjust VR3 until V.REF (pin 11 of CN3) equals -5 V.

2. Set the D/A channel 1 data register to 0 and adjust VR7 until the offset of D/A channel 1 (accessed through pin 32 of CN3) equals 0 V.

3. Set the D/A channel 0 data register to 0 and adjust VR6 until the output of D/A channel 0 (pin 30 of CN3) equals 0 V.